

CLAIMS

What is claimed is:

1 1. A processing block comprising:
2 a storage sub-block;
3 an execution sub-block to execute instructions; and
4 a thread management sub-block coupled to the storage and execution
5 sub-blocks, and equipped to store and maintain a thread switching structure in
6 the storage sub-block to facilitate interleaving execution of a plurality of threads
7 of instructions by the execution sub-block, with the thread structure including a
8 current thread identifier identifying one of the plurality of threads as a current
9 thread being currently executed by the execution sub-block, and a thread array of
10 thread entries, one per thread, correspondingly describing the plurality of
11 threads, each thread entry being created and added to the thread array by the
12 thread management sub-block as part of the execution of a create thread
13 instruction of a thread to spawn execution of another thread.

1 2. The processing block of claim 1, wherein each thread entry comprises a
2 thread program counter to identify an instruction of the corresponding described
3 thread as a current instruction to be executed, when the corresponding described
4 thread is being executed.

1 3. The processing block of claim 1, wherein each thread entry comprises an
2 activeness indicator indicating whether the corresponding described thread is
3 currently in an active state or an inactive state, where the corresponding
4 described thread is to be included among the threads to be interleavably

5 executed by the execution sub-block, while the thread is in the active state, and
6 not included, while the thread is in the inactive state.

1 4. The processing block of claim 3, wherein the thread management sub-
2 block is equipped to reset the activeness indicator of a thread from the active
3 state to the inactive state, as part of the execution of a thread termination
4 instruction of a thread terminating its own execution.

1 5. The processing block of claim 1, wherein each thread entry comprises
2 thread dependency information describing at least a plurality of registers of an
3 external set of registers, on which the corresponding described thread depends.

1 6. The processing block of claim 1, wherein the processing block further
2 comprises an interface to couple the processing block to an external set of
3 registers.

1 7. The processing block of claim 1, wherein the thread management sub-
2 block is further equipped to select a non-current one of the plurality of threads to
3 be the new current thread to be executed, updating the current thread identifier
4 and switching execution to a first instruction of the new current thread
5 accordingly, as part of the execution of a thread switching instruction of a thread
6 instructing the execution sub-block to switch execution to another thread.

1 8. The processing block of claim 7, wherein the execution sub-block is
2 equipped to select the next current thread on a selected one of a round-robin
3 basis, a fixed priority basis, and a rotating priority basis.

1 9. The processing block of claim 1, wherein the processing block further
2 comprises an input/output interface configurable to be a selected one of an input
3 interface and an output interface to particularize the processing block as a
4 selected one of an input processing block and an output processing block of a
5 signal processing macroblock.

1 10. The processing sub-block of claim 1, wherein the processing sub-block
2 further comprises another storage sub-block coupled to the execution sub-block,
3 to store instructions of the threads.

1 11. In a processing block, an execution method, comprising:
2 fetching a first instruction of a first thread of instructions; and
3 executing the first instruction, and as part of the execution of the first
4 instruction, adding a first thread entry in a thread array of a thread switching
5 structure, if the first instruction is a create thread instruction spawning interleaved
6 execution of a second thread of instructions with execution of other threads, the
7 thread switching structure being disposed and maintained within the processing
8 sub-block to facilitate interleaved execution of threads of instructions by the
9 processing sub-block, and the first thread entry describing the second thread.

1 12. The method of claim 11, wherein the first thread entry comprises a thread
2 program counter to identify an instruction of the second thread as a current
3 instruction to be executed, when the second thread is being executed.

1 13. The method of claim 11, wherein the first thread entry comprises an
2 activeness indicator indicating whether the second thread is currently in an active

3 state or an inactive state, where the second thread is to be included among the
4 threads to be interleavingly executed, while the second thread is in the active
5 state, and not included, while the second thread is in the inactive state.

1 14. The method of claim 11, wherein the first thread entry comprises thread
2 dependency information describing at least a plurality of registers of an external
3 set of registers, on which the second thread depends.

1 15. The method of claim 11, wherein said execution of the first instruction
2 includes resetting an activeness indicator of a second thread entry of the thread
3 array from indicating an active state to indicating an inactive state instead, if the
4 first instruction is a thread termination instruction terminating execution of the first
5 thread, the second thread entry being corresponding to the first thread.

1 16. The method of claim 11, wherein said execution of the first instruction
2 includes selecting the second thread from among a plurality of active threads,
3 updating a current thread identifier to identify the second thread as a new current
4 thread to be executed, replacing the first thread, and transferring execution to an
5 instruction of the second thread instead, if the first instruction is a thread
6 execution switching instruction, and execution of the second thread has
7 previously been spawned.

1 17. The method of claim 16, wherein said selection of the second thread from
2 among a plurality of active threads comprises selecting the second thread in a
3 selected one of a round-robin basis, a fixed priority basis, and a rotating priority
4 basis.

1 18. A signal processing macroblock comprising:
2 a set of registers; and
3 at least a selected one of
4 an input processing block coupled to the set of registers, including an
5 input interface, execution and thread management facilities
6 equipped to support interleaved execution of multiple threads of
7 instructions, and
8 an output processing block coupled to the set of registers, including an
9 output interface, execution and thread management facilities
10 equipped to support interleaved execution of multiple threads of
11 instructions.

1 19. The signal processing macroblock of claim 18, wherein the signal
2 processing macroblock further comprises a computation block coupled to the set
3 of registers, including execution and thread management facilities equipped to
4 support interleaved execution of multiple threads of instructions, including
5 instructions performing mathematical operations.

1 20. The signal processing macroblock of claim 19, wherein at least a selected
2 one of the facilities of the input processing block, the output processing block and
3 the computation block, equipped to support interleaved execution of multiple
4 threads, includes a storage sub-block to store a thread switching structure that
5 includes a current thread identifier identifying one of the multiple threads as a
6 current thread to be executed, and a thread array including thread entries
7 describing corresponding ones of the multiple threads.

1 21. The signal processing macroblock of claim 20, wherein at least a selected
2 one of the facilities of the input processing block, the output processing block and
3 the computation block, equipped to support interleaved execution of multiple
4 threads, further includes an execution sub-block equipped to create a thread
5 entry in the thread array for a thread as part of the execution of a create thread
6 instruction spawning interleaved execution of the thread.

1 22. The signal processing macroblock of claim 20, wherein at least a selected
2 one of the facilities of the input processing block, the output processing block and
3 the computation block, equipped to support interleaved execution of multiple
4 threads, further includes an execution sub-block equipped to reset an activeness
5 indicator of a thread entry in the thread array for a thread from indicating an
6 active state to indicating an inactive state as part of the execution of a thread
7 termination instruction terminating execution of the thread.

1 23. The signal processing macroblock of claim 20, wherein at least a selected
2 one of the facilities of the input processing block, the output processing block and
3 the computation block, equipped to support interleaved execution of multiple
4 threads, further includes an execution sub-block equipped to select a thread as a
5 new current thread to be executed, updating a current thread identifier of the
6 thread switching structure to identify the selected thread, and switching to
7 execute an instruction of the selected thread, as part of the execution of a thread
8 execution switching instruction.

1 24. A media processor comprising:
2 a direct memory access unit to access media data;

3 a plurality of signal processing units coupled to the direct memory access
4 unit to process the accessed media data, at least a first of which signal
5 processing units comprising
6 a set of registers,
7 an input processing block coupled to the set of registers, including an
8 input interface, execution and thread management facilities
9 equipped to support interleaved execution of multiple threads of
10 instructions, and
11 an output processing block coupled to the set of registers, including an
12 output interface, execution and thread management facilities
13 equipped to support interleaved execution of multiple threads of
14 instructions.

1 25. The media processor of claim 24, wherein the first signal processing unit
2 further comprises a computation block coupled to the set of registers, including
3 execution and thread management facilities equipped to support interleaved
4 execution of multiple threads of instructions, including instructions performing
5 mathematical operations.

1 26. The media processor of claim 25, wherein at least a selected one of the
2 facilities of the input processing block, the output processing block and the
3 computation block, equipped to support interleaved execution of multiple threads,
4 includes a storage sub-block to store a thread switching structure that includes a
5 current thread identifier identifying one of the multiple threads as a current thread
6 to be executed, and a thread array including thread entries describing
7 corresponding ones of the multiple threads.

1 27. The media processor of claim 25, wherein at least a selected one of the
2 facilities of the input processing block, the output processing block and the
3 computation block, equipped to support interleaved execution of multiple threads,
4 further includes an execution sub-block equipped to create a thread entry in the
5 thread array for a thread as part of the execution of a create thread instruction
6 spawning interleaved execution of the thread.

1 28. The media processor of claim 25, wherein at least a selected one of the
2 facilities of the input processing block, the output processing block and the
3 computation block, equipped to support interleaved execution of multiple threads,
4 further includes an execution sub-block equipped to reset an activeness indicator
5 of a thread entry in the thread array for a thread from indicating an active state to
6 indicating an inactive state as part of the execution of a thread termination
7 instruction terminating execution of the thread.

1 29. The media processor of claim 25, wherein at least a selected one of the
2 facilities of the input processing block, the output processing block and the
3 computation block, equipped to support interleaved execution of multiple threads,
4 further includes an execution sub-block equipped to select a thread as a new
5 current thread to be executed, updating a current thread identifier of the thread
6 switching structure to identify the selected thread, and switching to execute an
7 instruction of the selected thread, as part of the execution of a thread execution
8 switching instruction.

1 30. A system comprising:
2 a host processor;

3 first memory coupled to the host processor;
4 second memory;
5 a media processor coupled to the second memory and the host processor,
6 the media processor having at least
7 a direct memory access unit to access media data, and
8 a plurality of signal processing units coupled to the direct memory
9 access unit to process the accessed media, at least a first of which
10 signal processing units comprising
11 a set of registers,
12 an input processing block coupled to the set of registers,
13 including an input interface, execution and thread
14 management facilities equipped to support interleaved
15 execution of multiple threads of instructions, and
16 an output processing block coupled to the set of registers,
17 including an output interface, execution and thread
18 management facilities equipped to support interleaved
19 execution of multiple threads of instructions.

1 31. The system of claim 30, wherein the first signal processing unit of the
2 media processor further comprises a computation block coupled to the set of
3 registers, including execution and thread management facilitates equipped to
4 support interleaved execution of multiple threads of instructions, including
5 instructions performing mathematical operations.

1 32. The system of claim 31, wherein at least a selected one of the facilities of
2 the input processing block, the output processing block and the computation
3 block, equipped to support interleaved execution of multiple threads, includes a

4 storage sub-block to store a thread switching structure that includes a current
5 thread identifier identifying one of the multiple threads as a current thread to be
6 executed, and a thread array including thread entries describing corresponding
7 ones of the multiple threads.

1 33. The system of claim 31, wherein at least a selected one of the facilities of
2 the input processing block, the output processing block and the computation
3 block, equipped to support interleaved execution of multiple threads, further
4 includes an execution sub-block equipped to create a thread entry in the thread
5 array for a thread as part of the execution of a create thread instruction spawning
6 interleaved execution of the thread.

1 34. The system of claim 31, wherein at least a selected one of the facilities of
2 the input processing block, the output processing block and the computation
3 block, equipped to support interleaved execution of multiple threads, further
4 includes an execution sub-block equipped to reset an activeness indicator of a
5 thread entry in the thread array for a thread from indicating an active state to
6 indicating an inactive state as part of the execution of a thread termination
7 instruction terminating execution of the thread.

1 35. The system of claim 31, wherein at least a selected one of the facilities of
2 the input processing block, the output processing block and the computation
3 block, equipped to support interleaved execution of multiple threads, further
4 includes an execution sub-block equipped to select a thread as a new current
5 thread to be executed, updating a current thread identifier of the thread switching
6 structure to identify the selected thread, and switching to execute an instruction

7 of the selected thread, as part of the execution of a thread execution switching
8 instruction.

1 36. The system of claim 30, wherein the system is a selected one of a server,
2 a palm sized personal digital assistant, a wireless mobile phone, a set-top box,
3 an entertainment control console, a video recorder, or a video player.